REMARKS

(1) Claims 1-30 were pending in the present application. Claim 2 has been amended herein and claims 10-26 have been withdrawn. Accordingly, claims 1-9, and 27-30 are currently pending. No new matter has been added.

(2) Claim 2 has been objected to because of informalities. Claim 2 has been amended. The amendment has not narrowed the scope of the claim.

(3) The Examiner rejected claims 1-6, 8, 27-28, and 30 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,696,931 to Lum et al. (hereinafter "Lum"). Applicant respectfully traverses the section 102(b) rejection because Lum does not teach or suggest all of the limitations of the claims as originally submitted.

Claim 1 requires that the controller "calculates new cache counter and pointer values when the first requested data block is not contained within the first block of the cache." Lum does not disclose the calculation of a new cache counter and pointer values to permit access to data stored in blocks of a cache entry other than the initial block of the cache entry. Lum discloses that "the cache entry 390 is updated to reference the next sequential section stored in the disc cache, where the 'next sequential section' is the next sector after the last sector retrieved by the last Host Read Command. Instead of leaving the cache entry 390 unchanged after processing a Host Read Command, the present invention's disc controller's sequencer updates the cache entry 390 because further sequential accesses are more likely than repetitive accesses" (Column 7, Lines 42-50). Rather than "calculates new cache counter and pointer values when the first requested data block is not contained within the first block of the cache" as claim 1 requires,

Lum merely discloses the retrieval of data stored immediately after the data in the cache entry with the cache hit to replace the data stored in the cache entry. Accordingly, Applicant submits that claim 1 is patentable over Lum, and respectfully request withdrawal of the Examiner's rejection.

Claims 2-6 depend from claim 1. Applicant respectfully submits that these dependent claims are patentable over the cited prior art, not only because of their dependency from claim 1 for the reasons discussed above, but also in view of their novel claim features.

Claim 8 requires that "if a portion of the requested data is in the cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system **substantially concurrently** with transferring the portion of the requested data from the mass storage devices to the host system," (emphasis added). Claim 27 requires that "said logic means being operable to determine when a cache-hit-portion of data-blocks corresponding to said data-request reside in said cache and a cache-miss-portion of said data-blocks corresponding to said data-request do not reside in said cache, and operating in response to such a determination **to concurrently cause** said disk-controller to auto-transfer said cache-hit-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said cache-miss-portion of said data-request from said disk-device," (emphasis added) and claim 28 requires that "said logic circuit being operable to determine a partial-cache-hit when a first-portion of data-blocks corresponding to said data-request reside in said cache and a second-portion of said data-blocks corresponding to said data-request do not reside in said cache, and operating in response to a partial-cache-hit **to concurrently cause** said disk-controller to auto-transfer said first-portion of said data-blocks corresponding to said data-request from said cache,

and to cause said microprocessor to fetch data-blocks corresponding to said second-portion of said data-request from said disk-device" (emphasis added). Lum does not disclose transferring data from the cache to the host "substantially concurrently" with transferring data from the mass storage device to the host. Instead, Lum discloses "When the number of sequential sectors 304 requested by the host 102 is more than the number of sectors available in the disc cache buffer memory 118 (i.e., a partial cache hit) then the current sector count 200C in register 192 is decremented to zero during the initial data transfer of data from the disc cache 118 to the host 102. When the sequencer 130 detects that the current sector count 200C has reached zero, it stops the data transfer to the host 102 until the microprocessor 114 detects the status of the transfer, loads the remaining requested sectors into the buffer memory 118 and updates the next register 190 so that they can be transferred to the host 102" (Column 7, Lines 51-62). In other words, rather than a concurrent transfer, Lum merely teaches a **sequential** transfer of data from the cache to the processor, followed by a transfer of data from mass storage to cache and thence to the processor. Accordingly, Applicant submits that claims 8, 27, and 28 are patentable over Lum, and respectfully request withdrawal of the Examiner's rejection.

Claim 30 depend from claim 28. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 28 for the reasons discussed above, but also in view of its novel claim features.

(4) The Examiner rejected claims 7 and 29 under 35 U.S.C. § 103(a) as being unpatentable over Lum, in view of well-known practices in the art. Applicant respectfully traverses this rejection.

Claim 1 requires, *inter alia*, that the controller "calculates new cache counter and pointer values when the first requested data block is not contained within the first block of the cache." As discussed above, Lum does not teach or suggest this claim element. Examiner has not identified and Applicant is unaware of any well-know practices in the art, taken alone or in combination, that disclose the calculation of a new cache counter and pointer values to permit access to data within a cache entry when the first requested data block is not contained within the first block of the cache entry.

Claim 7 depends from claim 1. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 1 for the reasons discussed above, but also in view of its novel claim features.

Claim 28 requires, *inter alia*, that "said logic circuit being operable to determine a partial-cache-hit when a first-portion of data-blocks corresponding to said data-request reside in said cache and a second-portion of said data-blocks corresponding to said data-request do not reside in said cache, and operating in response to a partial-cache-hit **to concurrently cause** said disk-controller to auto-transfer said first-portion of said data-blocks corresponding to said data-request from said cache, and to cause said microprocessor to fetch data-blocks corresponding to said second-portion of said data-request from said disk-device" (emphasis added). As discussed above, Lum does not teach or suggest this element. Examiner has not identified and Applicant is unaware of any well-know practices that disclose the quoted claim limitation. Claim 29 depends from claim 28. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 28 for the reasons discussed above, but also in view of its novel claim features.

(5) The Examiner rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over Lum, in view of U.S. Patent Publication No. 2001/0014929 to Taroda et al. (hereinafter "Taroda"). Applicant respectfully traverses this rejection.

Claim 8 requires, *inter alia*, that "if a portion of the requested data is in the cache memory and a portion of the requested data is in the mass storage device, transferring the portion of the requested data from the cache memory to the host system **substantially concurrently** with transferring the portion of the requested data from the mass storage devices to the host system" (emphasis added). Neither Lum nor Taroda, taken alone or in combination, discloses the concurrent transfer of data from the cache and the mass storage device.

Claim 9 depends from claim 8. Applicant respectfully submits that this dependent claim is patentable over the cited prior art, not only because of its dependency from claim 8 for the reasons discussed above, but also in view of its novel claim features.

(6) In view of the above, Applicant respectfully submits that the application is in condition for allowance and request that the Examiner pass the case to issuance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Steven H. Slater, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible.

No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

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Steven H. Slater
Attorney for Applicant
Reg. No. 35,361

SLATER & MATSIL, L.L.P.
17950 Preston Rd.
Suite 1000
Dallas, Texas 75252
Tel.: 972-732-1001
Fax: 972-732-9218